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LISTING OF THE CLAIMS

In the Claims:

(Original) A data output circuit, comprising:

a plurality of registers;

a plurality of register output selection switches respectively connected to the plurality of registers via a plurality of first wires having first lengths, pairs of the plurality of register output selection switches being connected by respective common active regions;

a first data group selection switch that is connected to the common active regions of a first subset of the plurality of register output selection switches via a plurality of second wires having second lengths that are shorter than the first lengths;

a second data group selection switch that is connected to the common active regions of a second subset of the plurality of register output selection switches via a plurality of third wires having third lengths that are shorter than the first lengths, the first and second data group selection switches being disposed approximately a same distance from the first and second subsets of the plurality of register output selection switches, respectively; and

an output driver that is connected to the first and second data group selection switches.

- 2. (Original) The data output circuit of Claim 1, wherein the plurality of register output selection switches comprises a plurality of CMOS transmission gates, respectively.
 - (Original) A data output circuit, comprising:
 - a plurality of registers;
 - a plurality of register output selection switches respectively connected to the plurality of registers, pairs of the plurality of register output selection switches being connected by respective common active regions;
 - a first data group selection switch that is connected to the common active regions of a first subset of the plurality of register output selection switches;
 - a second data group selection switch that is connected to the common active regions of a second subset of the plurality of register output selection switches; and

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an output driver that is connected to the first and second data group selection switches.

- 4. (Original) The data output circuit of Claim 3, wherein the plurality of register output selection switches comprises a plurality of CMOS transmission gates, respectively.
 - 5. (Original) A data output circuit, comprising:
 - a plurality of registers;
- a plurality of register output selection switches respectively connected to the plurality of registers via a plurality of first wires having first lengths;
- a data group selection switch that is connected to the plurality of register output selection switches by a plurality of second wires having second lengths that are shorter than the first lengths; and

an output driver that is connected to the data group selection switch.

- 6. (Original) A data output circuit, comprising:
- a plurality of registers;
- a plurality of register output selection switches respectively connected to the plurality of registers;
- a first data group selection switch that is connected to a first subset of the plurality of register output selection switches via a first line having a first length;
- a second data group selection switch that is connected to a second subset of the plurality of register output selection switches via a second line having a second length that is approximately equal to the first length; and

an output driver that is connected to the first and second data group selection switches.

- 7. (Original) A data output circuit, comprising:
- a plurality of registers;
- a plurality of register output selection switches respectively connected to the plurality of registers and arranged in a circular configuration;

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a plurality of overlap prevention control signal lines respective ones of which are connected to pairs of the plurality of register output selection switches;

a data group selection switch that is connected to the plurality of register output selection switches; and

an output driver that is connected to the data group selection switch.